Abstract

A method and an apparatus to implement a flexible mechanism for enforcing coherency among caching structures have been disclosed. In one embodiment, the apparatus includes a translation-lookaside-buffer (TLB), a cache to provide temporary storage for a data block, and a memory management unit to implement a first cache-coherency mechanism if the processor is in a first mode and to implement a second cache-coherency mechanism if the processor is in a second mode. Other embodiments are described and claimed.